Claims

1. (Currently amended) A method of simulating a circuit, comprising:

reading a description of the circuit that includes a list of components in the circuit and the interconnections between the components, the circuit including both a first set of nodes and components responsive to time-domain signals, the time-domain signals comprising analog signals, and a second set of nodes and components responsive to time-frequency domain signals, the time-frequency domain signals comprising RF signals; and

in a single simulation flow, simulating ~~the~~ time-domain representations of signals on the first set of nodes and simulating ~~the~~ time-frequency domain representations of signals on the second set of nodes by solving two sets of equations until convergence, the two sets of equations including a first set of non-linear equations related to the time-domain signals and a second set of non-linear equations related to the time-frequency domain signals.

2. (Previously Presented) The method of claim 1, further comprising:

partitioning the circuit into at least one partition including one or more nodes and components from the first set and at least one partition including one or more nodes and components from the second set.

3.(Original) The method of claim 2, wherein the time-domain representations of signals are analog signals included in at least one analog partition and the time-frequency domain representations of signals are RF signals included in at least one RF partition and wherein a solution for simulation of the analog partition affects a solution for simulation of the RF partition.

4.(Previously Presented) The method of claim 1, further comprising receiving user input controlling how to partition the circuit and automatically refining the partitions to provide a higher probability of convergence.

5.(Previously Presented) The method of claim 1, further comprising partitioning the circuit based on user input and automatically sub-partitioning the circuit to increase simulation speed.

6.(Previously Presented) The method of claim 1, wherein simulating comprises solving each of the partitions separately and performing relaxations over all of the solved partitions.

7.(Previously Presented) The method of claim 1, further comprising:

partitioning the circuit into separate modules coupled together, with each module being associated with at least one boundary node external to the module;

positioning a boundary node by specifying the boundary node to a fixed value or spectrum; and

solving a partitioned module using the fixed value or spectrum assigned to the positioned boundary node.

8.(Original) The method of claim 1, wherein the time-domain representation of a signal is given by V(t) and the time-frequency domain representation of a signal is given by

$$v(t) = \sum_{k=-K}^{K} V_K(t) e^{j\omega_k(t)t}.$$

9.(Previously Presented) The method of claim 1, further comprising receiving, on a server computer, the description from a client computer over a distributed network, simulating the description on the server computer, and returning results to the client computer over the distributed network.

10.(Previously Presented) The method of claim 1, wherein simulating comprises solving analog and RF partitions for each time step H, and wherein the time step H is automatically adjusted based on the simulation results of previous time steps and input stimuli.

11. (Currently amended) A simulator apparatus for simulating a circuit, comprising:

a single simulator kernel including:

a) an analog solver simulating a first set of circuit nodes and components using time-domain representations of signals; and

b) an RF solver simulating a second set of circuit nodes and components using time-frequency domain representations of signals;

the simulator kernel solving, in a single simulation flow, a first set of non-linear equations related to the time-domain representations of signals and a second set of non-linear equations related to the time-frequency domain representations of signals so that solutions of the first set of equations affect solutions of the second set of equations and vice versa.

12.(Previously Presented) The simulator of claim 11, further comprising an input to read a netlist describing the physical characteristics of the circuit.

13.(Previously Presented) The simulator of claim 11, further comprising an input to receive control statements from a user to partition the circuit.

14.(Previously Presented) The simulator of claim 11, further comprising a partitioner to partition the first and second set of nodes and components into modules based on user input and to automatically sub-partition the modules to encourage convergence.

15.(Previously Presented) The simulator of claim 11, further comprising a relaxation tester coupled to the analog and RF solvers to perform one-step relaxation on results provided by the solvers.

16.(Previously Presented) The simulator of claim 11, further comprising an input to read an analog database and an RF database.

17.(Currently amended) A system for simulating a circuit, comprising:

means for reading a description of the circuit that comprises a list of components in the circuit and the interconnections between the components, the circuit comprising both a first set of nodes and

components responsive to time-domain signals, the time-domain signals comprising analog signals, and a second set of nodes and components responsive to time-frequency domain signals, the time-frequency domain signals comprising RF signals; and

means for simulating, in a single simulation flow, the first set of nodes using time-domain representations of signals and the second set of nodes using time-frequency domain representations of signals by using two sets of equations and solving the two sets in an interrelated manner until convergence.

18.(Previously Presented) The system of claim 17, further comprising a network and wherein the list is read from a client computer coupled to the network and the means for simulating includes a server computer coupled to the network.

19.(Previously Presented) The system of claim 17, further comprising means for partitioning based on user input and means for automatically sub-partitioning the circuit to provide a higher probability of convergence or to improve simulation speed.

20.(Previously Presented) The system of claim 17, further comprising analog solving means and RF solving means within a single simulator kernel.